REMARKS

The Office Action mailed on April 8, 2002, has been received and reviewed.

Claims 1 through 72 are currently pending in the application.

Claims 57 through 72 have been withdrawn from consideration as being directed to a non-elected invention. As claims 57 through 72 have been withdrawn from consideration, each of these claims has been canceled without prejudice or disclaimer.

Claims 1 through 56 are under consideration in the above-referenced application. Each of claims 1 through 56 stands rejected. Claims 4, 42, and 56 have been canceled without prejudice or disclaimer.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 103(a)

Claims 1 through 56 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,004,867 to Kim et al. (hereinafter "Kim") in view of U.S. Patent 5,990,546 to Igarashi et al. (hereinafter "Igarashi"), U.S. Patent 5,682,062 to Gaul (hereinafter "Gaul"), and U.S. Patent 5,229,647 to Gnadinger (hereinafter "Gnadinger").

The rejection is moot as to claims 4, 42, and 56, as each of these claims has been canceled without prejudice or disclaimer.

With respect to the claims that remain pending in the above-referenced application, it is respectfully submitted that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

Kim teaches chip-scale packages and methods for forming such chip-scale packages. The chip-scale packages of Kim include a semiconductor device, or die, and a substrate upon which terminals are located and by which electrical traces are carried. The terminals of the substrate are arranged correspondingly to the arrangement of bond pads on the semiconductor device. *See, e.g.*, FIG. 2. The substrate may include one or more layers of conductive traces. *See, e.g.*, FIG. 2; col. 3, lines 26-28; FIG. 3; col. 4, lines 47-51. The terminals and conductive traces are fabricated on an active surface of a semiconductor substrate, which ultimately becomes the bottom surface of the resulting substrate, by known semiconductor device fabrication processes. Col. 4, lines 13-18. Since conventional semiconductor device fabrication processes are used, material of the semiconductor substrate must be removed from the backside thereof, which ultimately becomes the top of the resulting substrate, so that terminals or other electrically conductive features may be exposed at both surfaces of the wafer. *See* FIG. 5D; col. 6, lines 19-21. As a consequence of the processes that are described in Kim, the teachigs of Kim are limited to substrates which have only terminals on their top surfaces (*i.e.*, the surfaces thereof that are to be positioned opposite, or away, from a semiconductor device.

Igarishi teaches a much different type of substrate that may be used in a chip-scale package. The substrate of Igarishi is a tape-automated bonding (TAB) type structure in which a routing conductor (*i.e.*, conductive traces) is sandwiched between two insulating layers. Col. 4, lines 38-45; FIGs. 1(A)-8. The teachings of Igarishi are limited to the use of a "metallic foil[-]laminated synthetic resin film" to form the substrate. Col. 5, lines 21-23. The substrate may be formed Terminals, or "electrodes", extend through both of the insulating layers to facilitate rerouting of the bond pads of a semiconductor device positioned adjacent to one side of the substrate to alternate locations on the opposite side of the substrate to provide the resulting chip-scale package with a desired connection pattern. Col. 4, lines 38-45; FIGs. 1(A)-8. Igarishi does not teach or suggest that conductive traces may be carried on a surface of the substrate. Rather, the teachings of Igarishi are limited to substrates with internally-extending conductive traces.

Gaul teaches semiconductor devices which have conductive vias extending from the active surfaces thereof to the backsides thereof. The conductive vias facilitate stacking the semiconductor devices and electrical connection of the stacked semiconductor devices to one another. Alternatively, the backsides of the semiconductor devices of Gaul may be positioned against substrates and the semiconductor devices electrically connected to the substrates by way of receptacles formed in or contact pads formed on the backsides of the semiconductor devices. *See* FIG. 4-G; col. 8, line 65, to col. 9, line 16; FIG. 6; col. 11, lines 20-41. Another package described in Gaul includes a thick overcoat of dielectric material formed over the active surface of a semiconductor device. The overcoat does not carry contacts, conductive traces, or any other conductive structures. In fact, Gaul lacks any teaching or suggestion of a substrate, such as an interposer, that carries contact pads and conductive traces and which is configured to be positioned adjacent to the active surface of a semiconductor device.

Gnadinger teaches a semiconductor device with through holes that extend partially through the thickness thereof. The through holes extend from conductively doped regions of silicon (diffusion regions 23) that are located beneath contact pads (*e.g.*, bond pads) on the active surface of the semiconductor device to the backside of the semiconductor device. Accordingly, when the semiconductor device is positioned over another, solder ball bearing semiconductor device with a through hole over a solder ball, during reflow of the solder, the solder may extend up into the through hole and contact a diffusion region 23, which communicates electrically with the overlying contact pad. In this manner, electrical connection may be established between or by way of the two adjacent semiconductor devices.

It is respectfully submitted that a *prima facie* case of obviousness under 35 U.S.C § 103 of the pending claims of the above-referenced application cannot be established based merely on the teachings of Kim, Igarishi, Gaul, and Gnadinger.

First, it is respectfully submitted that, one of ordinary skill in the art would not have been motivated to combine the teachings of these references in the manner that has been asserted. In particular, it is respectfully submitted that, while Kim teaches the use of a substrate formed from

silicon, there is no teaching or suggestion in any of Kim, Igarishi, Gaul, Gnadinger, and the knowledge that was generally available in the art to have modified Kim in such a way as to provide at least one conductive trace on a surface of a substrate that comprises silicon which is opposite from the surface of the substrate that is configured to be positioned adjacent to a semiconductor device, as recited in each of the pending claims of the above-referenced application. In this regard, Kim teaches that material must be removed from the backside of a wafer upon which a substrate is formed (*i.e.*, the upper surface of the substrate) following assembly of the substrate with a semiconductor device to expose electrodes at the upper surface of the substrate. FIG. 5D; col. 6, lines 19-21. Although Igarishi teaches a method for forming a substrate, that method is applicable to the formation of TAB type substrates, not substrates that are formed on silicon wafers, as taught in Kim. Gaul and Gnadinger likewise lack any teaching or suggestion that would be applicable to the formation of conductive traces on a surface of a semiconductor-comprising substrate which is to face away from a corresponding semiconductor device. Accordingly, it is respectfully submitted that any motivation to modify the teachings of Kim or to combine the teachings any of Igarishi, Gaul, and Gnadinger with those of Kim could only have been improperly based on the benefit of hindsight provided solely by the teachings of the Applicant's above-referenced application.

Second, it is respectfully submitted that a *prima facie* case of obviousness under 35 U.S.C. § 103 has not been established because none of Kim, Igarishi, Gaul, or Gnadinger, taken either alone or in combination, teaches or suggests each and every element of any of claims 1 through 3, 5 through 41, or 43 through 55.

Independent claim 1, as amended and presented herein, recites a chip-scale package which includes a semiconductor device and a substrate disposed adjacent an active surface of the semiconductor device. The substrate comprises a semiconductor material. At least one electrically conductive via extends at least partially through the substrate and communicates with a corresponding bond pad of the semiconductor device. In addition, at least one conductive trace

is carried on a surface of the substrate which is opposite from the surface of the substrate that is adjacent to the semiconductor device.

None of Kim, Igarishi, Gaul, or Gnadinger teaches or suggests a chip-scale package which includes a substrate with a conductive trace carried on a surface thereof which is opposite from the surface of the substrate that is positioned adjacent to a semiconductor device. Instead, the conductive traces of the substrates that are taught in Kim and Igarishi are internally confined. Gaul and Gnadinger lack any detail with respect to substrates.

It is, therefore, respectfully submitted that, under 35 U.S.C. § 103(a), amended independent claim 1 is allowable over Kim, Igarishi, Gaul, and Gnadinger.

Claims 2, 3, and 5 through 20 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Claim 13 is further allowable because none of Kim, Igarishi, Gaul, or Gnadinger teaches or suggests that a surface of a substrate which faces away from a semiconductor device may be at least partially coated with an oxide.

Claim 14 is further allowable because none of Kim, Igarishi, Gaul, or Gnadinger teaches or suggests that a surface of a substrate which faces away from a semiconductor device may be at least partially coated with a silicon oxide.

Claim 16 is additionally allowable since Kim, Igarishi, Gaul, and Gnadinger each lack any teaching or suggestion of a chip-scale package with an intermediate layer which comprises an adhesive material between the semiconductor device and substrate thereof.

Claim 17 is also allowable since all of Kim, Igarishi, Gaul, and Gnadinger fail to teach or suggest a chip-scale package that includes an intermediate layer comprising polyimide between the semiconductor device and substrate thereof.

Claim 20 is further allowable because Kim, Igarishi, Gaul, and Gnadinger neither teach or suggest a chip-scale package with a contact comprising a diffusion region between at least one electrically conductive via of the substrate thereof and a corresponding bond pad of the semiconductor device thereof, or that such a diffusion region may comprise a bond pad material

and a via material. Rather, the diffusion region taught in Gnadinger is a conductively doped area of silicon.

Independent claim 21, as amended and presented herein, also recites a chip-scale package that includes a substrate and a semiconductor device. The substrate of amended independent claim 21 comprises semiconductor material and includes a first surface with contact areas that are arranged correspondingly to an arrangement of bond pads on the semiconductor device, as well as conductive vias extending therethrough and a second surface carrying at least one conductive trace that extends laterally from a conductive via. Amended independent claim 21 also recites that bond pads of the semiconductor device communicate through corresponding conductive vias of the substrate.

As none of Kim, Igarishi, Gaul, or Gnadinger teaches or suggests a chip-scale package which includes a substrate that includes a first surface with contact areas that are arranged correspondingly to an arrangement of bond pads of semiconductor device and a second surface carrying at least one conductive trace that extends laterally from a conductive via through the substrate, it is respectfully submitted that Kim, Igarishi, Gaul, and Gnadinger do not teach or suggest each and every element of amended independent claim 21.

Therefore, it is respectfully submitted that, under 35 U.S.C. § 103(a), amended independent claim 21 is allowable over Kim, Igarishi, Gaul, and Gnadinger.

Each of claims 22 through 42 is allowable, among other reasons, as depending either directly or indirectly from claim 21, which is allowable.

Claim 24 is further allowable since none of Kim, Igarishi, Gaul, or Gnadinger teaches or suggests a diffusion region comprising a bond pad material and a conductive via material between a bond pad and a conductive via.

Claim 28 is additionally allowable because Kim, Igarishi, Gaul, and Gnadinger each lack any teaching and suggestion of a chip-scale package that includes an intermediate layer

comprising a material which adheres the semiconductor device of the package to the substrate of the package.

Claim 29 depends from claim 26 and is also allowable since none of Kim, Igarishi, Gaul, and Gnadinger teaches or suggests a chip-scale package which includes an intermediate layer that comprises a polyimide.

Claim 39 is further allowable because none of Kim, Igarishi, Gaul, or Gnadinger teaches or suggests that a surface of a substrate which faces away from a semiconductor device may be at least partially coated with an oxide.

Claim 40 is further allowable because none of Kim, Igarishi, Gaul, or Gnadinger teaches or suggests that a surface of a substrate which faces away from a semiconductor device may be at least partially coated with a silicon oxide.

Independent claim 43, as amended and presented herein, recites a flip-chip carrier. The flip-chip carrier of independent claim 43 includes a substrate that comprises semiconductor material. The substrate includes at least one via formed therethrough. A first end of the via is located proximate a first surface of the substrate and is positioned to substantially align with a corresponding bond pad of a semiconductor device to be assembled with the substrate. The substrate also includes at least one conductive trace laterally extending from a second end of the at least one via and carried by a second surface of the substrate.

Again, Kim, Igarishi, Gaul, and Gnadinger each lack any teaching or suggestion of a substrate with a first end of at least one via being positioned proximate a first surface so as to substantially align with a corresponding bond pad of a semiconductor device and at least one conductive trace carried by a second surface of the substrate and extending laterally from a second end of the via. As none of Kim, Igarishi, Gaul, or Gnadinger, taken either alone or in combination, teaches or suggests each and every element of amended independent claim 43, it is respectfully submitted that, under 35 U.S.C. § 103(a), amended independent claim 43 is allowable over each of these references.

Claims 44 through 55 are each allowable, among other reasons, as depending either directly or indirectly from claim 43, which is allowable.

Claim 46 is further allowable because none of Kim, Igarishi, Gaul, or Gnadinger teaches or suggests that a surface of a substrate may be at least partially coated with an oxide. Rather, Kim teaches that an oxide may be formed on the active surface of a semiconductor device. Col. 3, lines 1-4.

Claim 47 is further allowable because none of Kim, Igarishi, Gaul, or Gnadinger teaches or suggests that a surface of a substrate may be at least partially coated with a silicon oxide. Again, the teachings of Kim are limited to providing such a layer on a semiconductor device, not on a substrate. Col. 3, lines 1-4.

Claim 53 is additionally allowable since Kim, Igarishi, Gaul, and Gnadinger each lack any teaching or suggestion of a flip-chip carrier that includes an adhesive layer disposed adjacent to as surface thereof.

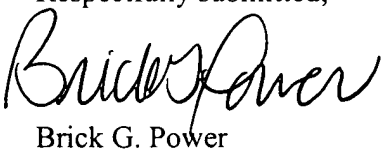
Claim 54, which depends from claim 53, is also allowable since none of Kim, Igarishi, Gaul, or Gnadinger teaches or suggests an adhesive layer which comprises a polyimide.

For these reasons, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 1 through 3, 5 through 41, and 43 through 55 be withdrawn.

CONCLUSION

It is respectfully submitted that each of claims 1 through 3, 5 through 41, and 43 through 55 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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Enclosure: Version with Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended) A chip-scale package, comprising:

a semiconductor device including an active surface; and

a [semiconductor] substrate comprising a semiconductor material disposed adjacent said active surface and including:

at least one electrically conductive via extending at least partially therethrough and being in communication with a corresponding bond pad of said semiconductor device; and

at least one conductive trace carried on a surface of said substrate which is opposite from another surface of said substrate that is adjacent to said semiconductor device.

2. (Amended) The chip-scale package of claim 1, further comprising an electrically conductive bump protruding from said [semiconductor] substrate opposite said semiconductor device and in communication with said at least one electrically conductive via.

3. (Twice amended) The chip-scale package of claim 1, wherein said substrate comprises at least [one] another electrically conductive via that extends substantially directly [through said semiconductor substrate] therethrough.

5. (Amended) The chip-scale package of claim 1, wherein a substrate of said semiconductor device and said [semiconductor] substrate comprising semiconductor material comprise the same type of semiconductor material.

6. (Amended) The chip-scale package of claim 1, wherein a substrate of said semiconductor device and said [semiconductor] substrate comprising semiconductor material comprise materials having substantially the same coefficients of thermal expansion.

8. (Amended) The chip-scale package of claim 1, wherein said semiconductor [substrate] material comprises silicon.

9. (Amended) The chip-scale package of claim 1, wherein a first thickness of said semiconductor device and a second thickness of said [semiconductor] substrate are substantially the same.

10. (Amended) The chip-scale package of claim 1, wherein a first thickness of said semiconductor device is greater than a second thickness of said [semiconductor] substrate.

11. (Amended) The chip-scale package of claim 1, wherein [a] said another surface of said [semiconductor] substrate [located opposite said semiconductor device comprises] is at least partially coated with an insulative material.

15. (Amended) The chip-scale package of claim 1, further comprising an intermediate layer disposed between said semiconductor device and said [semiconductor] substrate.

21. (Amended) [The] A chip-scale package, comprising:

a [semiconductor] substrate comprising semiconductor material and including:

a first surface with contact areas arranged correspondingly to an arrangement of bond pads on an active surface of a semiconductor device of the chip-scale package;

conductive vias extending therethrough and corresponding to said contact areas; and

a second surface carrying at least one conductive trace extending laterally from a conductive via of said conductive vias; and

[a] said semiconductor device invertedly disposed adjacent said [semiconductor] substrate so that [at least one] bond [pad] pads of said semiconductor device [communicates] communicate through [a] corresponding [via] conductive vias of said [semiconductor] substrate.

22. (Amended) The chip-scale package of claim 21, wherein said [at least one] bond [pad contacts] pads contact said corresponding [via] conductive vias.

23. (Amended) The chip-scale package of claim 22, further comprising [a] diffusion [region] regions between said [at least one] bond [pad] pads and said corresponding [via] conductive vias.

24. (Amended) The chip-scale package of claim 23, wherein each of said diffusion [region] regions comprises a bond pad material and a via material.

25. (Amended) The chip-scale package of claim 24, wherein said diffusion [region] regions at least partially [secures] secure said semiconductor device to said [semiconductor] substrate.

26. (Amended) The chip-scale package of claim 21, further comprising an intermediate layer disposed between said [semiconductor] substrate and said semiconductor device.

27. (Amended) The chip-scale package of claim 26, wherein said [at least one] bond [pad] pads and said corresponding [via] vias contact each other through said intermediate layer.

28. (Amended) The chip-scale package of claim 26, wherein said intermediate layer comprises a material which adheres said semiconductor device to said [semiconductor] substrate.

30. (Amended) The chip-scale package of claim 21, further comprising [a] at least one conductive bump in communication with at least one conductive via of said corresponding [via] conductive vias and protruding from said [semiconductor] substrate opposite from said semiconductor device.

31. (Amended) The chip-scale package of claim 30, wherein said at least one conductive bump comprises solder.

32. (Amended) The chip-scale package of claim 21, wherein said [semiconductor] substrate comprising semiconductor material and a substrate of said semiconductor device comprise the same material.

33. (Amended) The chip-scale package of claim 21, wherein said [semiconductor] substrate comprises silicon.

35. (Amended) The chip-scale package of claim 21, wherein a first thickness of said [semiconductor] substrate and a second thickness of said semiconductor device are substantially equal.

36. (Amended) The chip-scale package of claim 21, wherein a first thickness of said [semiconductor] substrate is less than a second thickness of said semiconductor device.

37. (Amended) The chip-scale package of claim 21, further comprising an insulative material disposed on at least a portion of said second [a] surface of said [semiconductor] substrate[opposite said semiconductor device].

38. (Amended) The chip-scale package of claim 37, wherein at least one conductive via of said corresponding [via] conductive vias is exposed through said insulative material.

41. (Amended) The chip-scale package of claim 37, wherein said insulative material comprises an insulative layer disposed substantially over said second surface.

43. (Twice amended) A flip-chip carrier, comprising a [semiconductor] substrate comprising semiconductor material and including:

at least one via formed therethrough and having a first end located proximate a first surface of said substrate and positioned to substantially align with a corresponding bond pad of a semiconductor device to be assembled with said [semiconductor] substrate; and

at least one conductive trace laterally extending from a second end of said at least one via and carried by a second surface of said substrate.

45. (Amended) The flip-chip carrier of claim 43, further comprising an insulative material disposed on at least a portion of at least one surface of said [semiconductor] substrate.

50. (Amended) The flip-chip carrier of claim 43, wherein said [semiconductor] substrate comprises silicon.

51. (Twice amended) The flip-chip carrier of claim 43, further comprising a conductive bump disposed adjacent an end of said at least one conductive trace located opposite from said second end of said at least one via.

53. (Amended) The flip-chip carrier of claim 43, further comprising an adhesive layer disposed adjacent [a] said first surface of said [semiconductor] substrate.

55. (Amended) The flip-chip carrier of claim 53, wherein [an] said first end of said at least one via extends through said adhesive layer.